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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,487	08/20/2003	Hiroyuki Ishizaki	P/1071-1598	7400
2352	7590	12/29/2005	EXAMINER	
OSTROLENK FABER GERB & SOFFEN 1180 AVENUE OF THE AMERICAS NEW YORK, NY 100368403			PATEL, ISHWARBHAI B	
			ART UNIT	PAPER NUMBER
			2841	

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/644,487

Applicant(s)

ISHIZAKI, HIROYUKI

Examiner

Ishwar (I. B.) Patel

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 September 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) 3-5,9 and 10 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2 and 6-8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>9/28/05</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on September 28, 2005 has been entered.

2. Applicant is advised that the Notice of Allowance mailed on April 7, 2005 is vacated in view of the Request for the Continued Examination filed along with an Information Disclosure Statement (IDS). If the issue fee has already been paid, applicant may request a refund or request that the fee be credited to a deposit account. However, applicant may wait until the application is either found allowable or held abandoned. If allowed, upon receipt of a new Notice of Allowance, applicant may request that the previously submitted issue fee be applied. If abandoned, applicant may request refund or credit to a specified Deposit Account.

Rejections based on the newly cited reference(s) (references from the newly filed IDS) follow.

Election/Restrictions

3. Applicant's election of specie I, reading on figure 1-2, claims 1, 2 and 6-8 in the reply filed on March 11, 2005 is acknowledged and reinstated. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Priority

4. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been received and filed and placed of record in the file.

Claim Rejections - 35 USC § 103

5. Claims 1, 2 and 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art of Bentlage et al., Japanese Patent application NO. 08-330358 (Bentlage), in view of Hirano, Japanese Patent Application No. 09-260435 (Hirano).

Regarding claim 1, Bentlage, in figure 7, discloses mounting board comprising: a base substrate (22) having a first principal surface; a wiring electrode (58, figure 8) formed on the first principal surface of the base substrate; and an insulation film (54) which partially covers the first principal surface of the base substrate and the wiring electrode, the insulation film having a coated portion where the base substrate and the

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wiring electrode are coated with the insulation film, and an opening portion where the base substrate and the wiring electrode are not coated with the insulation film (see figure 7).

Bentlage does not explicitly disclose the relation $L/T \geq 2$ is satisfied, where L denotes the minimum width of a portion of the base substrate exposed at the opening portion and T denotes the thickness of the insulation film. However, Bentlage, in the prior figures 1-5, with related description, with more detail in figure 5, discloses that a void may remain while filling encapsulant in the narrow gap between the insulating film (mask) and the solder joint, (marked as void 42 in figure 5). Bentlage, in the invention remove this narrow gap to avoid the chances of void during filling of the encapsulant. This shows that the minimum width of a portion of the base substrate exposed is quite larger to have enough spacing to avoid void.

Hirano, in figure 1(a) and 1(b), discloses mounting board, with base substrate (11) with wiring electrode (15) and insulating layer (13, 14), partially covering the principal surface of the base substrate and the wiring electrode with an opening portion where the base substrate and the wiring electrode are not coated in insulating film (area between the insulating layer (13,14). Hirano further recites that the thickness of the insulating layer is such that the gap between the chip bottom and the top of the resin should enough for filling the resin with a filler, preferably no smaller than the 1.5 times the filler. This will equally applicable to the gap between the connection joint (joint between the electrodes 15 and 17 and the insulating layer 13 and 15).

A person of ordinary skill in the art at the time of applicant's invention would have been motivated to increase the gap (the minimum width of a portion of the base substrate exposed at the opening portion) in combination of the thickness of the insulating material, in order to have enough spacing, to have reliable and void free filling of the resin having filler. Further, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the structure of Bintlage, with the claimed limitation, as taught by Hirano, in order to have reliable and void free resin filling.

Regarding claim 2, the modified structure of Bintlage further discloses the opening portion straddles the wiring electrode and thereby forms a recess on each side of the wiring electrode (Hirano, figure 1 and 2, Bintlage figure 7 and 8).

Regarding claim 6, modified structure of Bintlage discloses an electronic device comprising: the mounting board according to claim 1, as applied to claim 1 above; an electronic component (26, figure 11) having a bump electrode (37) formed so as to correspond to the wiring electrode (58, 24) in the opening portion, via which the electronic component is mounted on the mounting board, and a gap between the first principal surface of the base substrate and the electronic component being filled with

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sealing resin, the electronic component mounted on the mounting board by connecting the bump electrode with a portion of the wiring electrode exposed at the opening portion or the uncoated portion of the mounting board; and the sealing resin (encapsulant) filled and hardened in a gap between the first principal surface of the base substrate and the electronic component.

6. Claims 7 and 8 rejected under 35 U.S.C. 103(a) as being unpatentable over the modified structure of Bentlage as applied to claim 6 above, and further in view of Yamada et al., US Patent No. 5,959,363 (Yamada) and Thompson et al., US Patent No. 5,218,234 (Thompson).

Regarding claim 7 and 8, the modified structure of Bentlage discloses all the features of claimed invention as applied to claim 6 above, including the sealing resin filled and hardened in a gap between the first principal surface of the base substrate and the electronic component, as applied to claim 6 above, but does not disclose said sealing resin has a viscosity range of 0.02 to 10 Pa.s before hardening, as claimed in claim 7 and said viscosity range is 0.4 to 7.3 Pa.s, as claimed in claim 8.

Yamada, in the background discussion recites, if the viscosity of a resin is higher, it will make impossible to fill the resin into the space between the semiconductor chip and the wiring board and if the viscosity of a resin is too low, the resin may excessively spread over a wide range of area around a semiconductor chip, column 4, line 52-67.

Thompson, in the background discussion recites that one of the controlling factor to regulate the unwanted flow of epoxy resin is to control the viscosity of the resin, column 1, line 60-65.

A person of ordinary skill in the art would have been motivated to control the desired viscosity of the resin material for a reliable underfilling the gap between the semiconductor chip and the wiring board (substrate).

Therefore, it would have obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the modified structure of Bentlage with the resin having the viscosity as claimed in claim 7 and 8, as taught by Yamada and Thompson, in order to have reliable underfilling the gap between the semiconductor chip and the substrate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Ishwar (I. B.) Patel
Examiner
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December 26, 2005